ELEN0037
Microelectronic IC Design

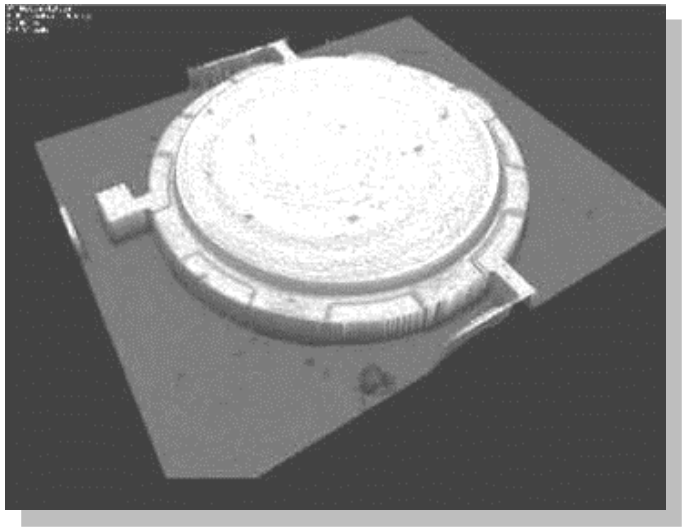
Prof. Dr. Michael Kraft

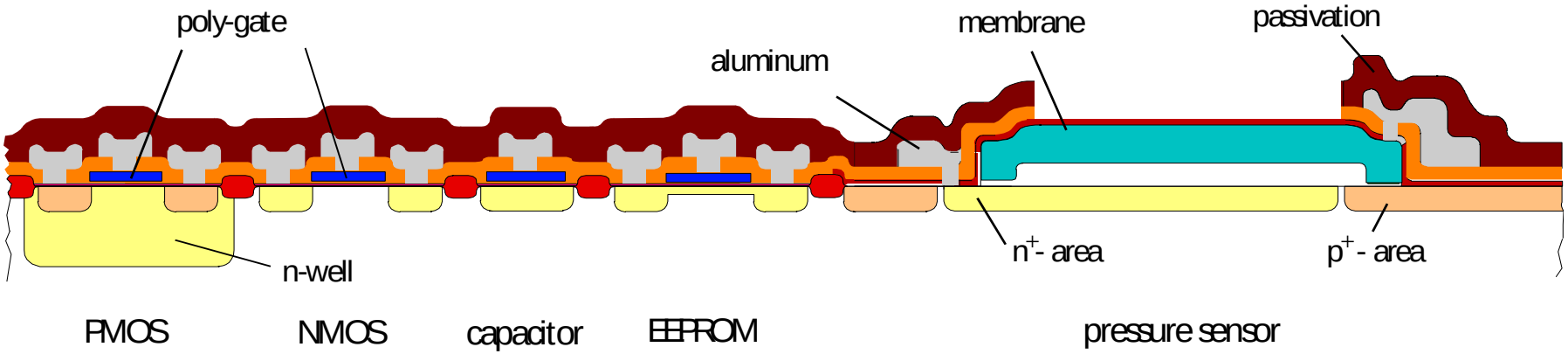
Lecture 2:
Technological Aspects

- Technology
  - Passive components
  - Active components
  - CMOS Process
- Basic Layout
- Scaling

CMOS Technology

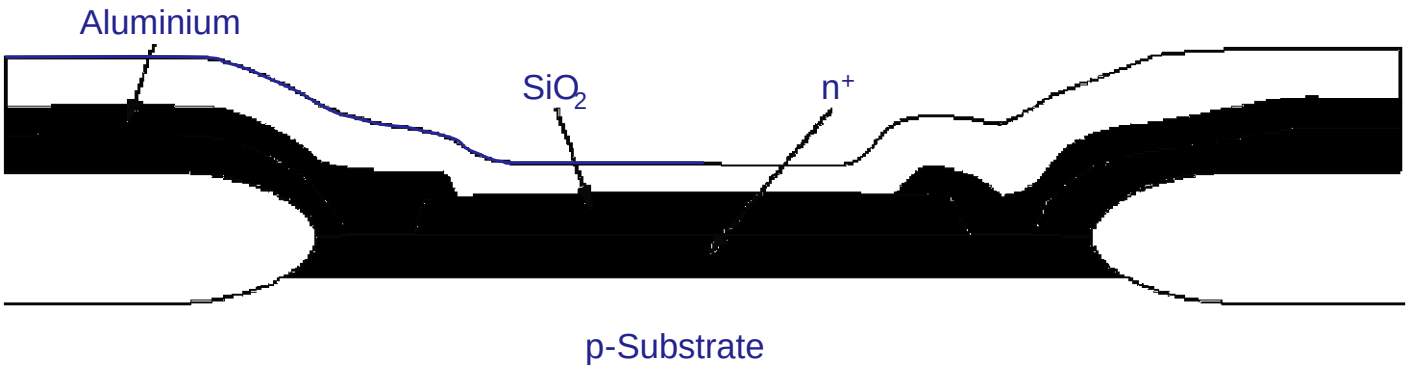
- Integrated capacitive pressure sensor on 8“ wafer using surface micromachining
- → Integrated single chip solution





Passive Components

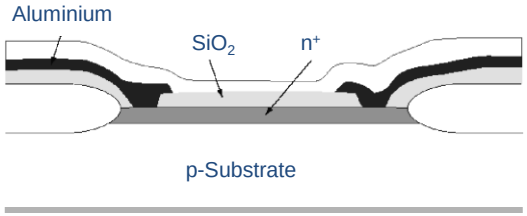
- Passive components:
  - Resistors
    - Diffused/implanted resistors
    - Polysilicon resistors
  - Capacitors



n+ diffusion resistor

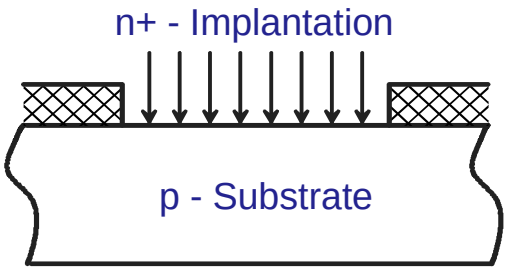
Source: Allen, Holberg, „CMOS Analog Circuit Design“

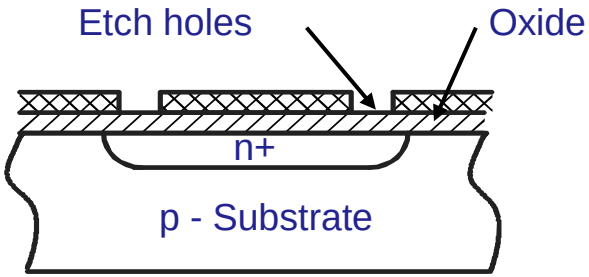
Fabrication n+ Diffusion Resistor

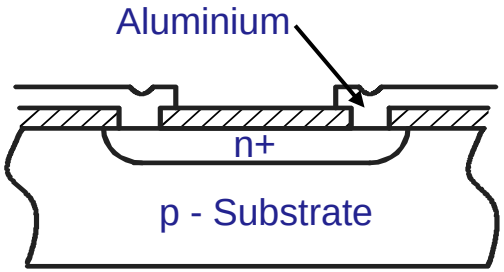


- Diffusion Resistor:
  - Source/Drain diffusion

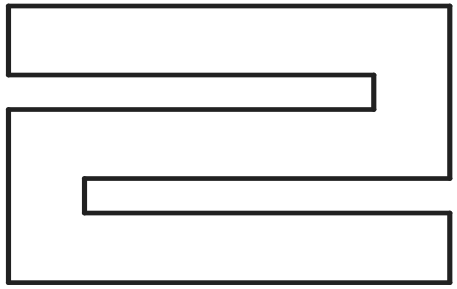
Fabrication process

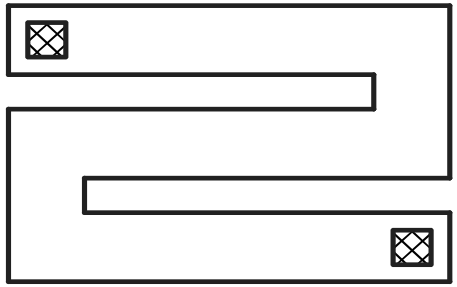






Mask layout





n+ Diffusion Resistor

- Specific conductivity $\sigma = q(\mu_n n + \mu_p p)$

  $n >> p$

  $\Rightarrow \sigma \approx q\mu_n n = q\mu_n N_D$

- Resistance

$$R = \frac{1}{\sigma}\frac{L}{A} = \frac{1}{\sigma \cdot X_j}\frac{L}{W}$$

$$R = \frac{1}{q\mu_n N_D X_j}\frac{L}{W}$$

$$R_{\blacksquare} = \frac{1}{q\mu_n N_D X_j}$$ ="Square Resistance"

σ: specific conductivity

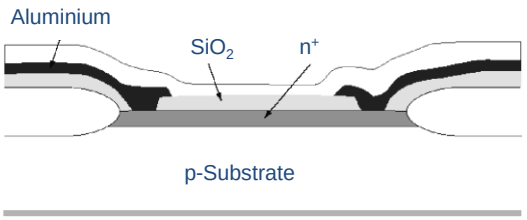
μ_n, μ_p: charge mobility

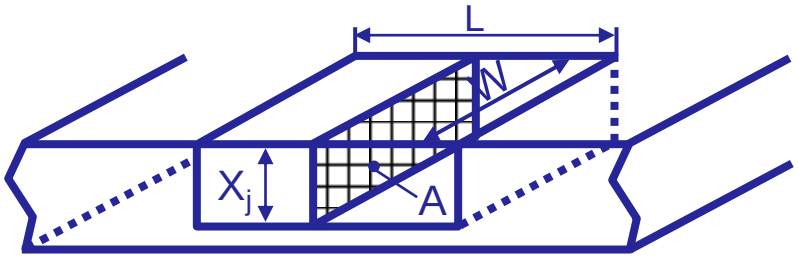
X_j: p-n junction depth

n,p: charge concentration

$\frac{L}{W}$: Geometry factor

N_D, N_A: donor, acceptor concentration





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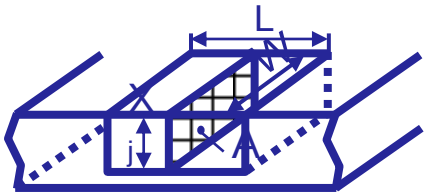

- Resistance

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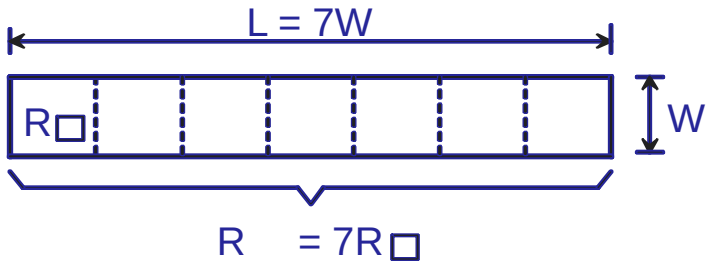
μ_n, μ_p: charge mobility
X_j: p-n junction depth
n,p: charge concentration
$\frac{L}{W}$: Geometry factor
N_D, N_A: donor, acceptor concentration

- Square resistance only depends on process parameters
  - *L=W* → *R□ = R*
  - Resistors are specified as multiples of their square resistance

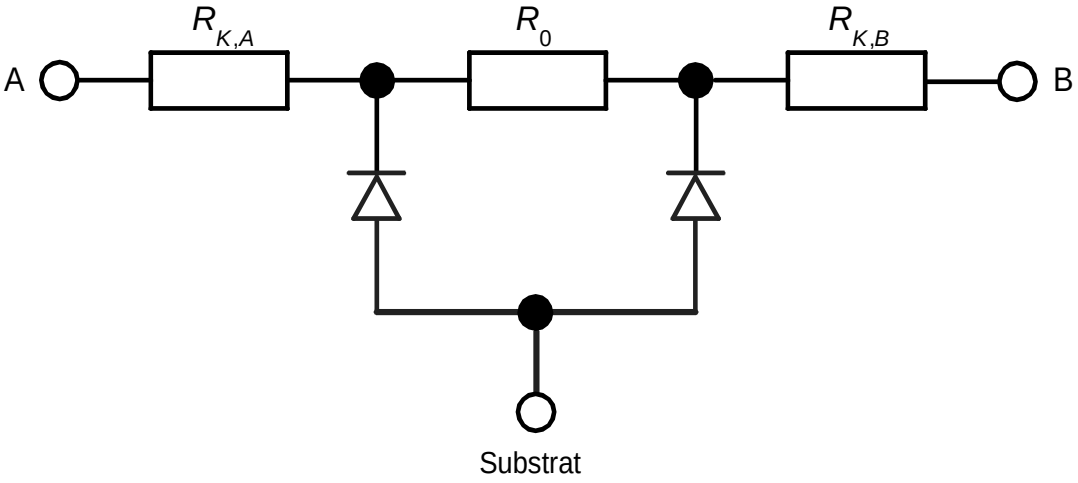


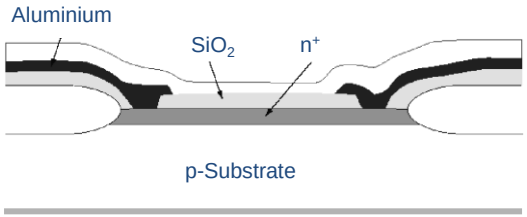
n+ Diffusion Resistor

- Typical values for *R□:*
  - Drain-source regions: 10..100 Ω/□
  - N-well: 1000…10000 Ω/□
- Absolute values for diffusion resistors
  - N_D, X_j, μ_n depend on process parameter
    - Diffusion concentration
    - Implantation dose
    - Diffusion temperature
    - Diffusion time
    - etc
  - *W, L* depend on lithography, etch process, lateral diffusion, etc
    - Edge definition has tolerance of $\Delta L, \Delta W \approx 0.1 \mu m$
  - → high tolerance for absolute values of resistance, 10-50%

- For high resistance values, large areas are required

Electrical Equivalent Model





- Contact resistances (R_k) add to resistance value
- Parasitic diode (pn-junction) to substrate → leakage currents, voltage dependent depletion layer capacitance,

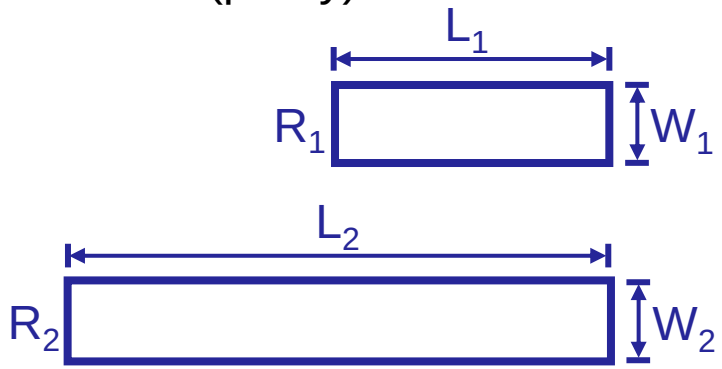
Resistor Matching

- How accurate can a resistor **ratio** be fabricated
- Example: $R_2 = 2\ R_1$

$$\frac{R_1}{R_2} = \frac{N_{D2} X_{j2} \mu_{n2}}{N_{D1} X_{j1} \mu_{n1}} \cdot \frac{L_1}{L_2} \cdot \frac{W_2}{W_1} \approx \frac{L_1 W_2}{L_2 W_1}$$

$\frac{N_{D2} X_{j2} \mu_{n2}}{N_{D1} X_{j1} \mu_{n1}}$ Depend on the process, so should be (pretty) equal across a wafer

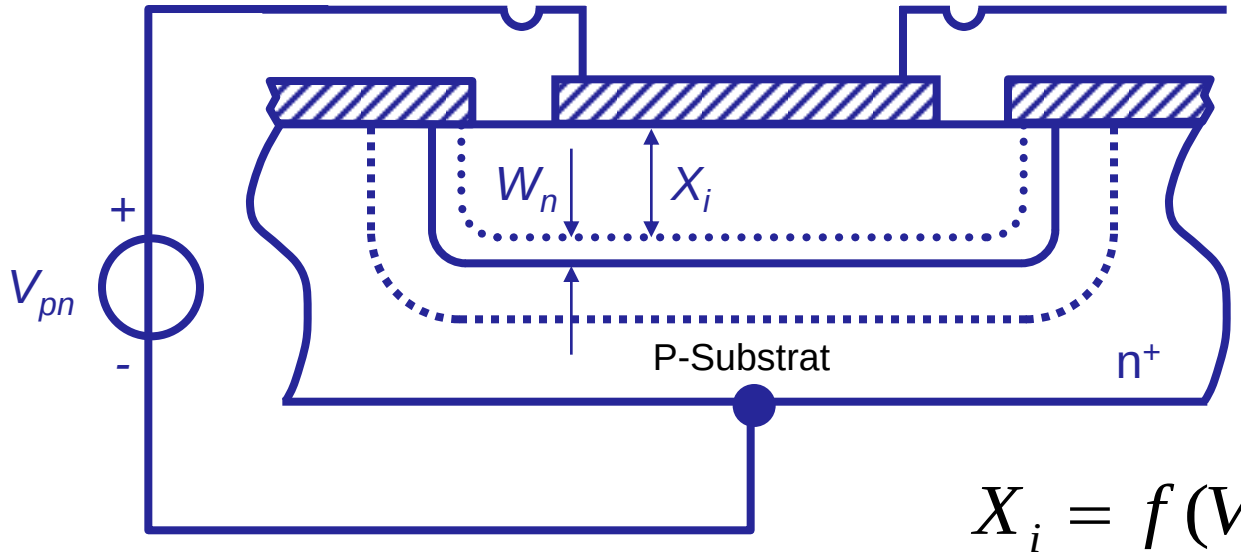
$\frac{L_1}{L_2} \cdot \frac{W_2}{W_1}$ Depend on the geometry



- If the resistors are fabbed in the same process,
- and are close together
- → process tolerances cancel out!
- → with "good" layout the matching can be better than 1‰
- → for circuit design better use ratios!

Voltage Dependence Diffusion Resistance

- Depletion zone width, W_n depends on junction reverse voltage bias, V_{pn}



$$X_i = f(V_{pn})$$

$$W_n = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V_{pn})}$$

$$X_i(V_{pn}) = X_i(V_{pn} = 0) - W_n(V_{pn})$$

- → Resistance increases with junction reverse voltage bias

Example

$$X_i(0) = 0.1\mu m$$

$$N_A = 1.8 \cdot 10^{14} cm^{-3}$$

$$N_D = 10^{19} cm^{-3}$$

$$V_{bi} = 0.74V$$

$$W_n(V_{SP} = 0) = 4 \cdot 10^{-5}\ \mu m$$

$$W_n(V_{pn} = 10V) = 1.6 \cdot 10^{-4}\ \mu m$$

$$\Delta X_i \approx -1.6 \cdot 10^{-4}\ \mu m$$

$$\frac{\Delta X_i}{X_i} = -1.6 \cdot 10^{-3} \Rightarrow \frac{\Delta R}{R} = 1.6 \cdot 10^{-3}$$

Voltage Coefficient Diffusion Resistance

$$\frac{1}{R}\cdot\frac{\Delta R}{\Delta V}=1.6\cdot10^{-4}V^{-1}=160\,ppm/V$$

- Voltage dependency increases with:
  - Lower doping
  - Higher square resistance
  - Thinner layers
- Typical values
  - n+ implantation: 20 Ω/☐ 100ppm/V
  - p+ implantation: 100 Ω/☐ 1100ppm/V
  - n- Implantation: 8 kΩ/☐ 20000 ppm/V

Temperature Dependency Diffusion Resistance

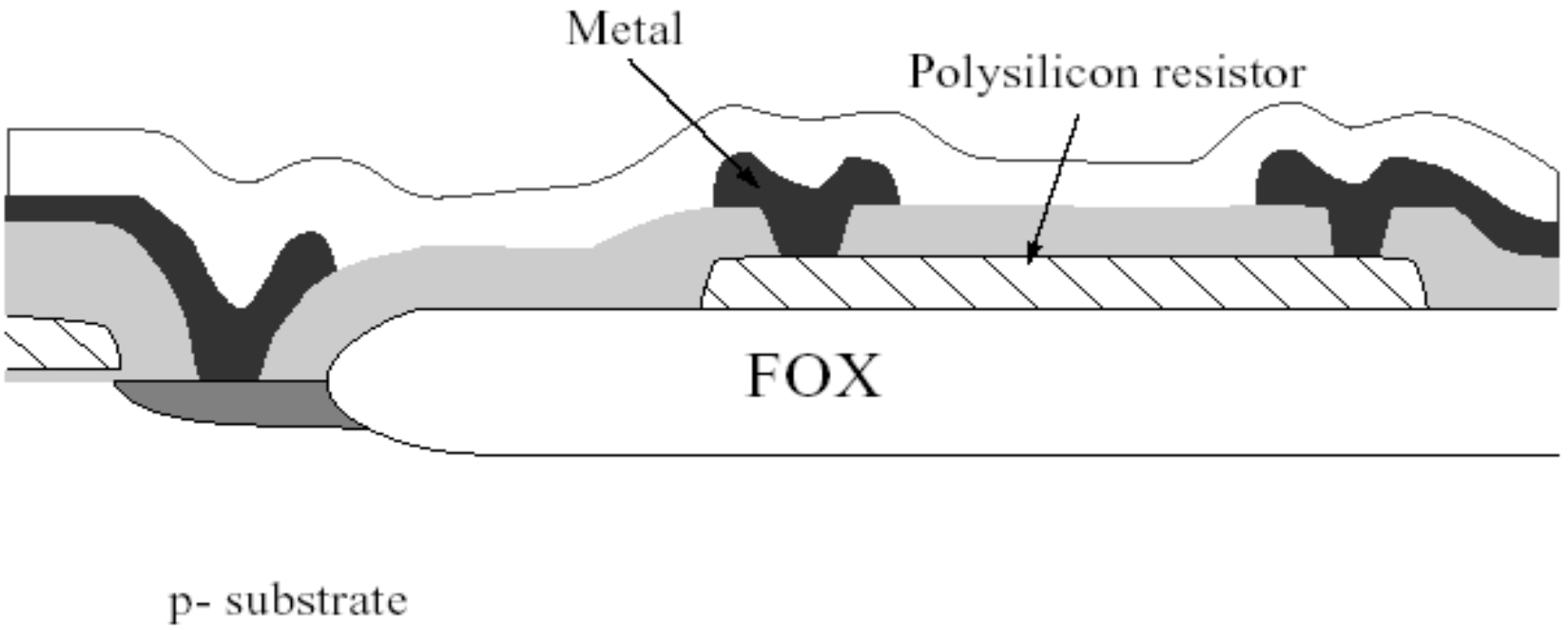
- Effective mobility is temperature dependent

$$\mu = f(T) \quad \frac{\mu}{\mu_0} = \left(\frac{T}{T_0}\right)^{-m}; \quad m = f(N_D, N_A)$$

$$\Rightarrow \frac{R}{R_0} = \left(\frac{T}{T_0}\right)^{m} \quad \frac{1}{R} \cdot \frac{\Delta R}{\Delta T} = \frac{m}{T} = TK_R$$

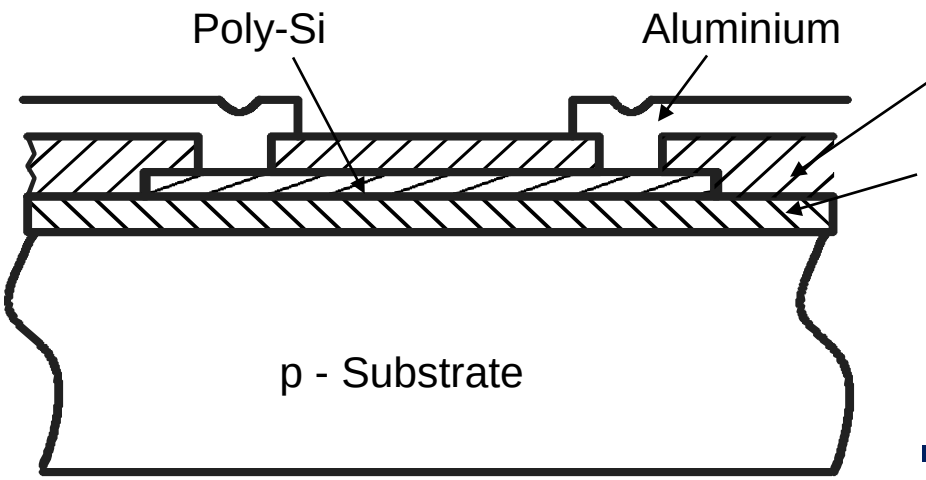
- m depends on various scattering mechanisms
- Temperature dependence decreases for higher doping levels
- Typical values:
  - n+ implantation: 20 Ω/☐ 1500ppm/K
  - n- implantation: 8 kΩ/☐ 8000ppm/K

Polysilicon Resistors



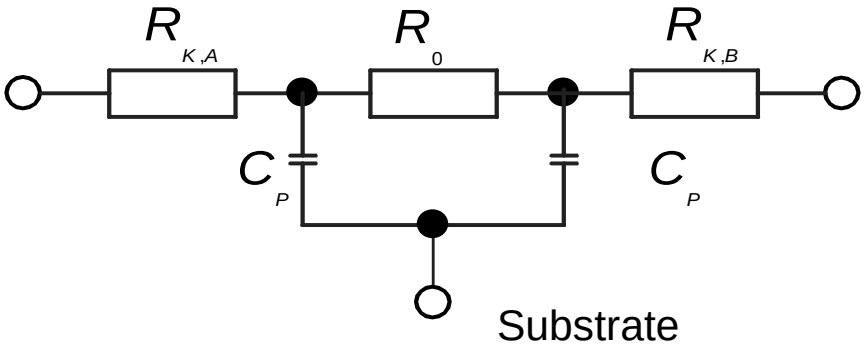
Polysilicon Resistors

- highly doped polycrystalline silicon
  - used a Gate material, interconnects



doping concentration $(typ.10^{20} cm^{-3})$

Electrical equivalent circuit:



- Current is nonlinear due to grain boundaries

$$I = I_s \cdot \sinh\left(\frac{eL_K}{2kTL} \cdot V\right)$$

  - L: resistor length
  - L_k: grain length, typ. 20..50nm
    - Relatively good linearity

Voltage Dependency Polysilicon Resistors

$$\frac{1}{R} = \frac{dl}{dV} = l_s \frac{eL_K}{2kTL} \cosh\left(\frac{eL_k}{2kTL} V\right)$$

$$\frac{1}{R}\frac{dR}{dV} = \frac{1}{V}\left\{1 - \frac{eL_K V}{2kTL} \coth\left(\frac{eL_K V}{2kTL}\right)\right\}$$

$$\approx -\frac{1}{3}\left(\frac{eL_K}{2kTL}\right)^2 V$$

- Long resistors have better linearity
  - Typ. Value 10..100 ppm/V
  - e.g. W=25 μm, L=2500 μm → 30 ppm/V

Temperature Dependency Polysilicon Resistors

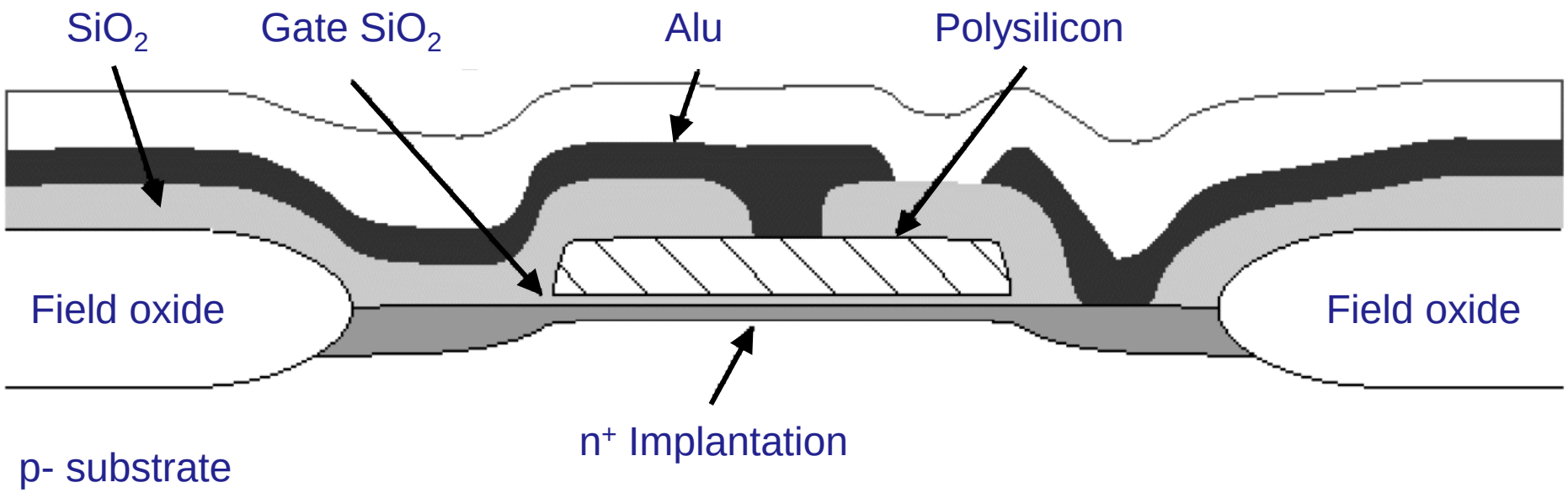
$$\frac{1}{R}\frac{dR}{dT} = \frac{1}{T}\left\{1 - \frac{eL_K V}{2kTL}\coth\left(\frac{eL_K V}{2kTL}\right)\right\}$$

$$\approx \frac{1}{3T}\left(\frac{eL_K V}{2kTL}\right)^2$$

- Long resistors have lower temperature dependency
  - Typ. Value 100..500 ppm/K
  - e.g. L=300 μm, V=2 V → 200 ppm/K

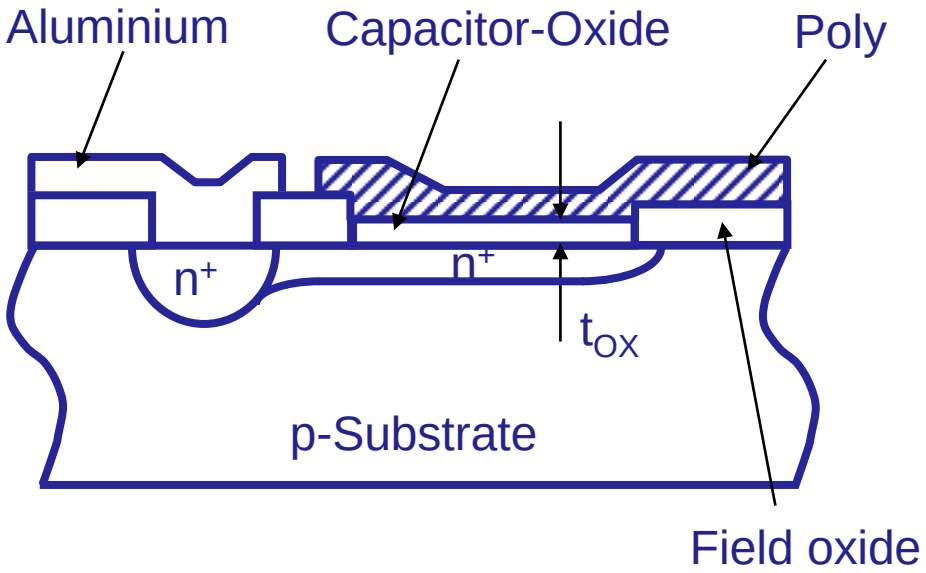
Capacitors

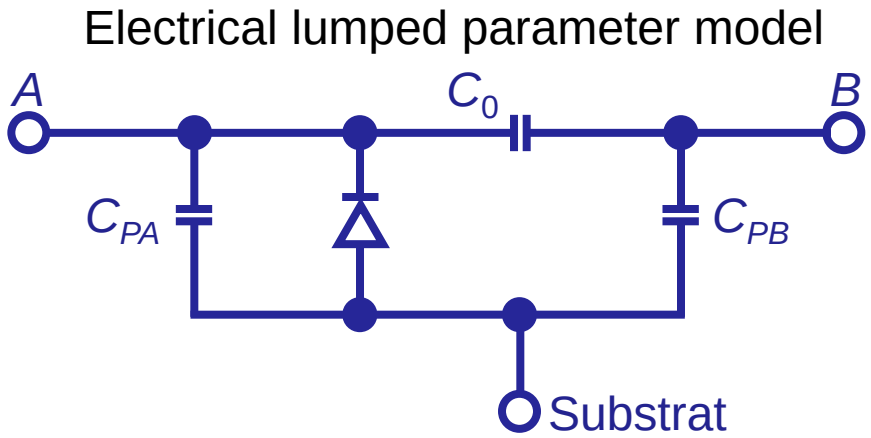
- CMOS technology:
  - High quality, thin gate oxide layers are available
  - Using MOSFET, one can realize switches with low losses
  - Using MOSFET, one can read-out stored voltages without (almost) losses



Poly Diffusion Capacitor

- CMOS technology:
  - High quality, thin gate oxide layers are available
    - Thickness 5..50 nm (Field oxide about factor 10 thicker)
  - Using MOSFET, one can realize switches with low losses
  - Using MOSFET, one can read-out stored voltages without (almost) losses





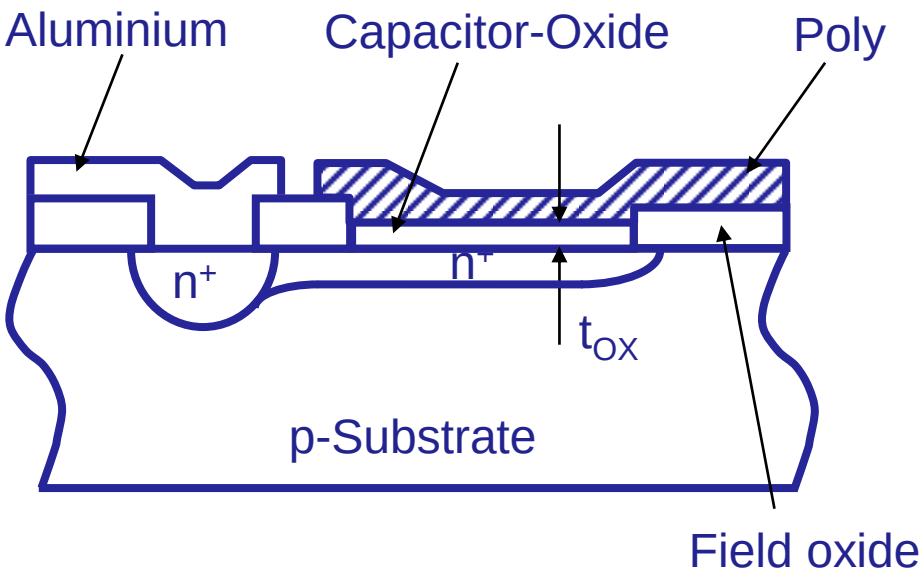
$$C_O = \frac{\varepsilon_0 \varepsilon_{r,SiO_2}}{t_{OX}} A = C_{ox} A = C_{ox} WL$$

Poly Diffusion Capacitor

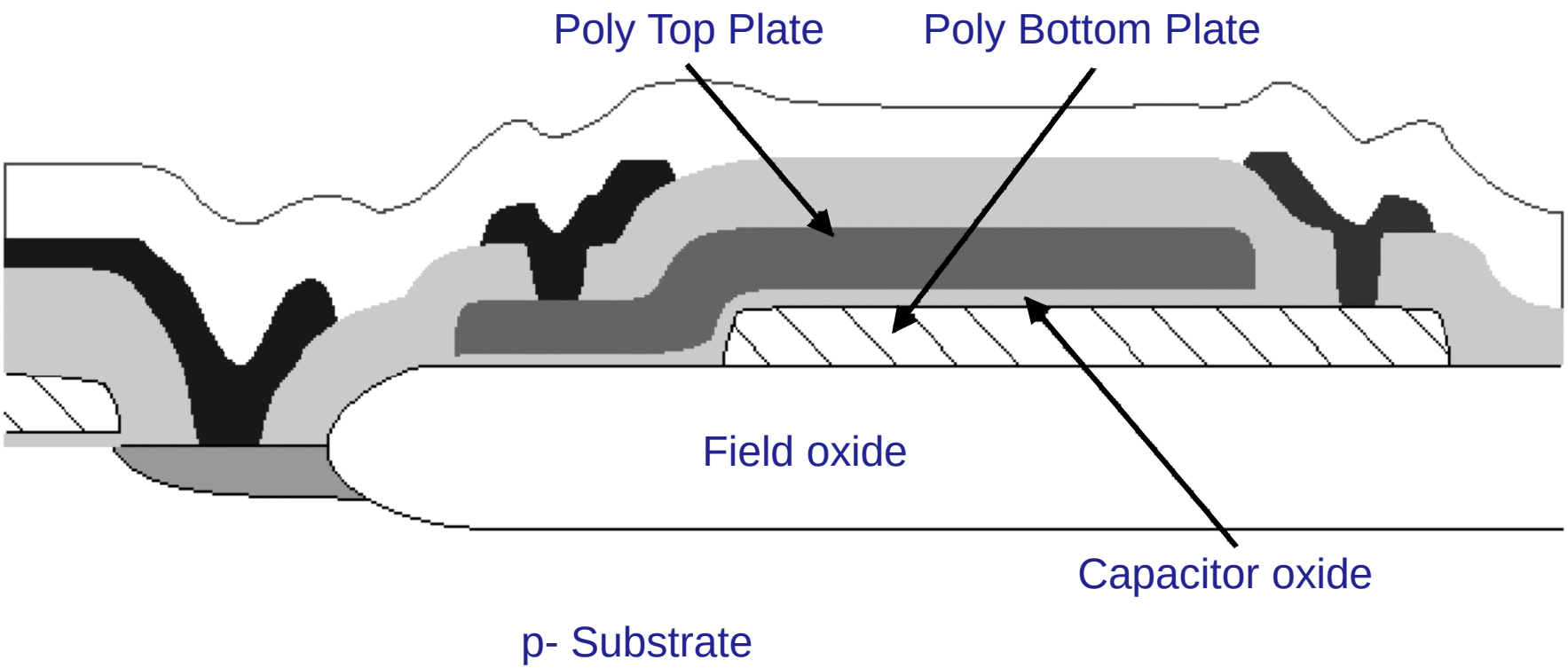
- C* depends on the process only
  - Typical values 500 pF/mm² .. 1.5 nF/mm²
- Small temperature and voltage dependency
- Absolute accuracy 10%..20%
- Matched pairs accuracy < 0.1%
- Disadvantage: diode to substrate

$$\frac{1}{C}\frac{dC}{dT} \approx 20\,ppm/K$$

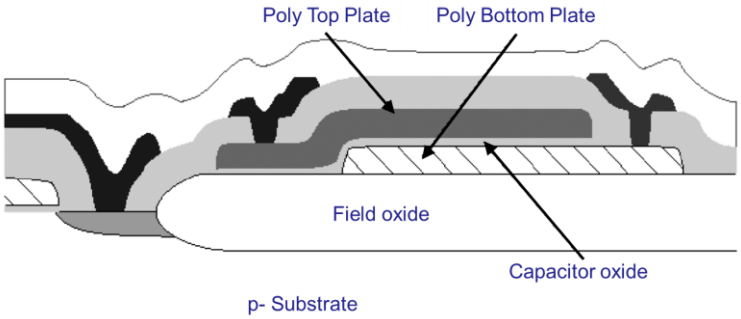
$$\frac{1}{C}\frac{dC}{dV} \approx 7\,ppm/V$$

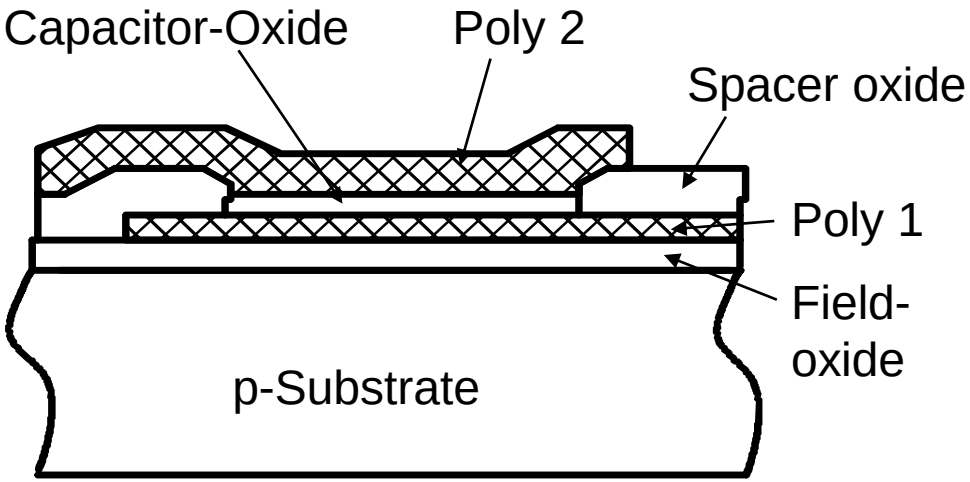


Poly-Poly Capacitor

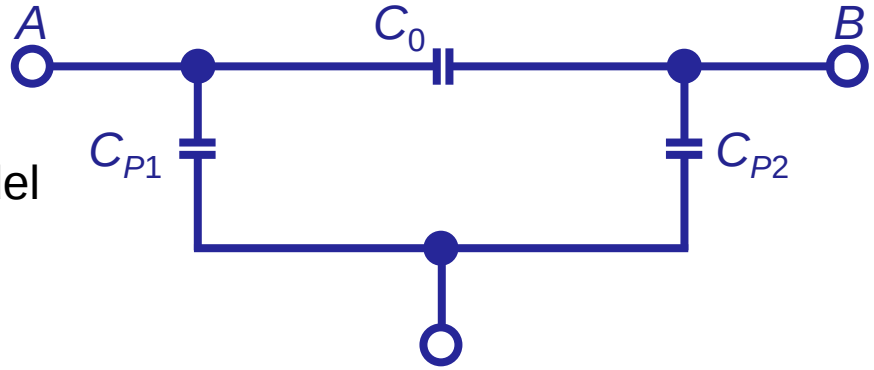


Poly-Poly Capacitor





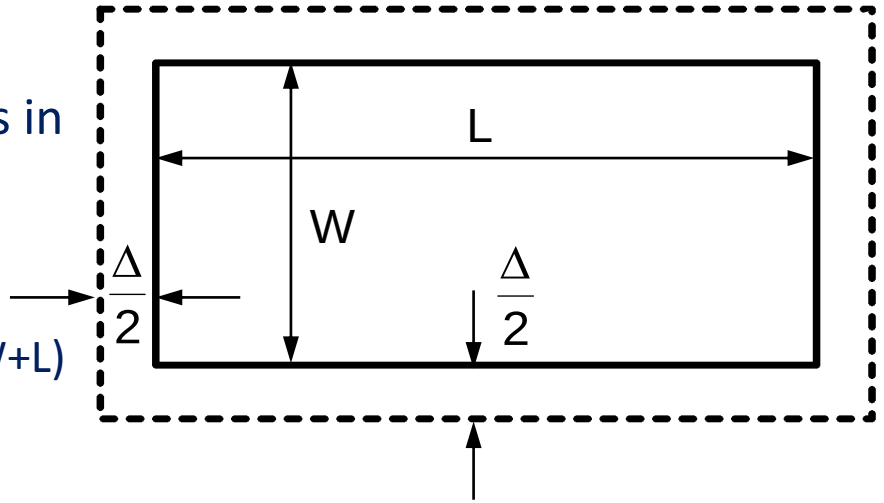
Electrical lumped parameter model



$$C_0 = \frac{\varepsilon_0 \varepsilon_{r,Sio_2}}{t_{OX}} \cdot A = C_{ox} \cdot A = C_{ox} \cdot W \cdot L$$

Poly-Poly Capacitor Absolute Value

- Source of tolerances
  - 1. Edge uncertainty due to tolerances in
    - Lithography
    - Etching
  - → W+Δ and L+Δ
    - Area A = WL, circumference U = 2 (W+L)



$$A` = (W+\Delta)(L+\Delta) = WL + \Delta(W+L) + \Delta^2$$

$$A' = A + \Delta\frac{U}{2} + \Delta^2 \approx A + \Delta\frac{U}{2}$$

$$\frac{A'-A}{A} = \Delta\frac{U}{2A}$$

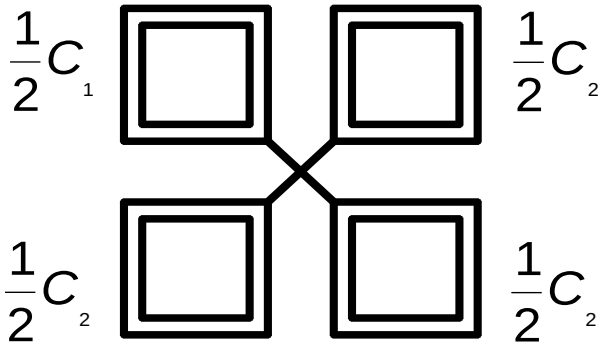
  - → minimal error for minimum ratio U to A
    - → quadratic layout (best spherical)
  - 2. oxide thickness
    - Process dependent

Capacitors: Matching

- Area and circumference have to adjusted
  - Required capacitor value build up from quadratic unit capacitors
- Oxide thickness changes across a wafer (gradient)
  - Common centroid layout

- parasitic capacitors
  - Electrodes to substrate
  - Interconnect
  - Fringe field and stray capacitors
    - Can be in the same order as C_0
    - Circuit should be insensitive

example:



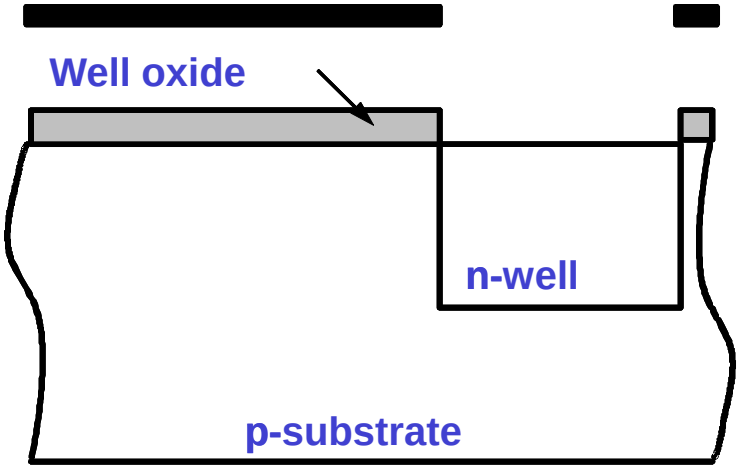
$$C_0 = \frac{\varepsilon_0 \varepsilon_{r,SiO_2}}{t_{OX}} \cdot A = C_{ox} \cdot A = C_{ox} \cdot W \cdot L$$

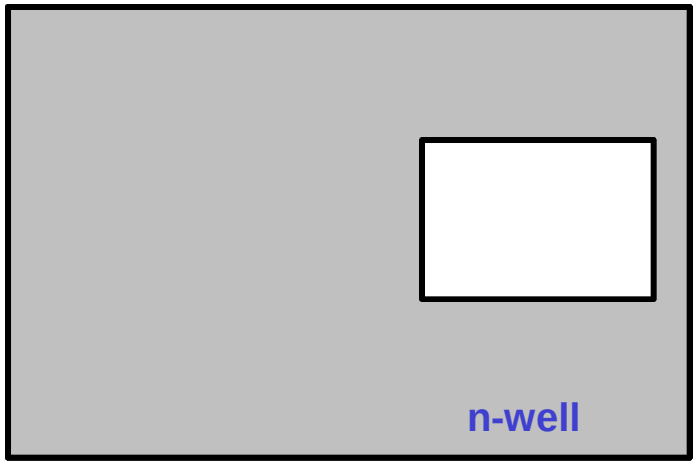
Precision of Passive Components

	Diffusion Resistor	Thinfilm Resistor	Capacitor
Absolute	10 – 50 %	≤ 1 %	10 – 30 %
Matching	0.05 – 0.1 % (9 – 10 bit)	0.01 - 0.1 % (9 – 12 bit)	0.02 – 0.3 % (7 – 11 bit)
Temperature Coefficient	2000 ppm/K	100 ppm/K	25 ppm/K
Voltage coefficient	(100 – 500) ppm/V	≤ 1 ppm/V	10 – 100 ppm/V

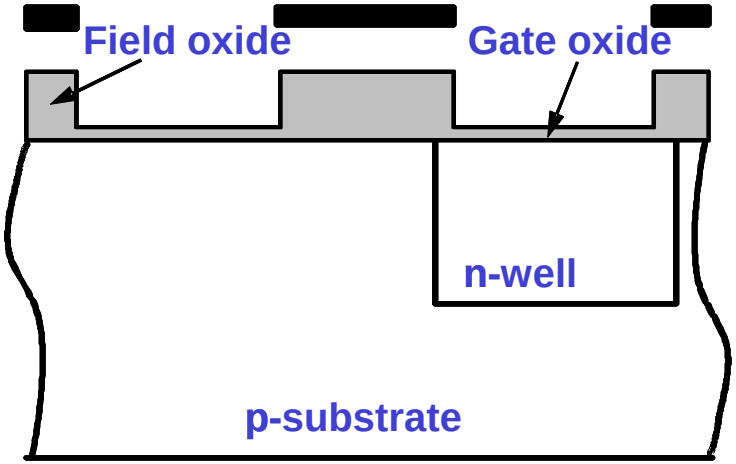
MOSFET Fabrication

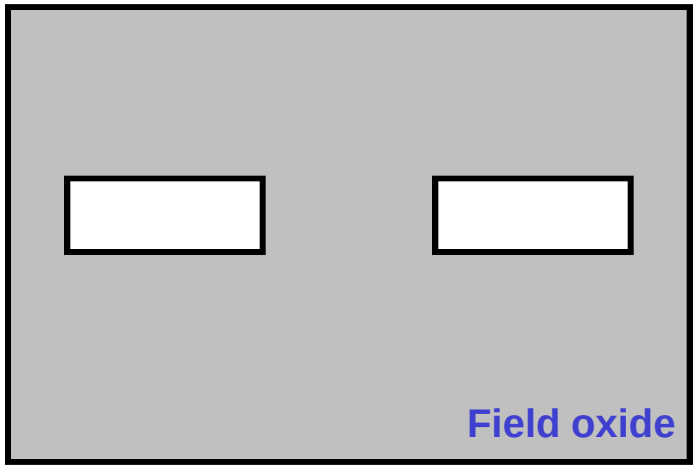
a) n-well





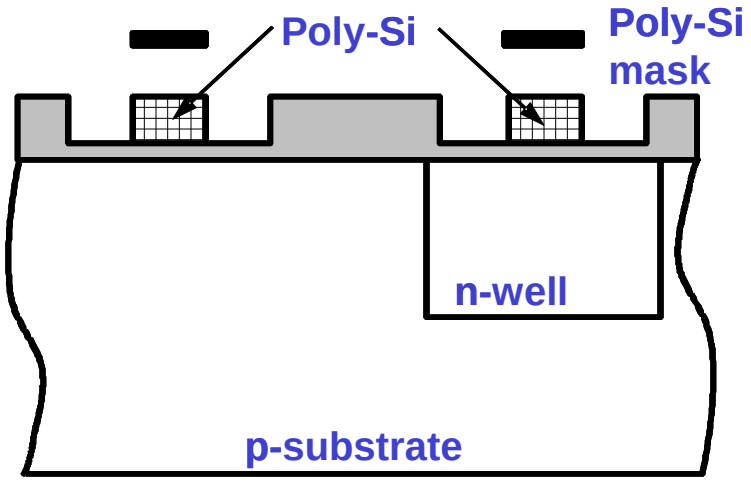
b) Aktive areas

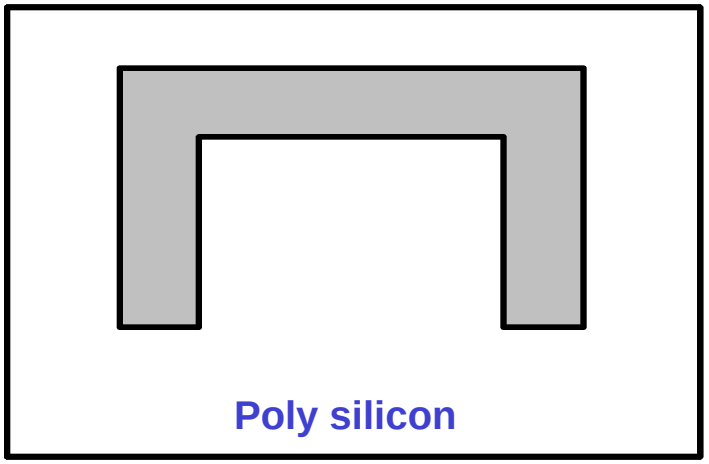




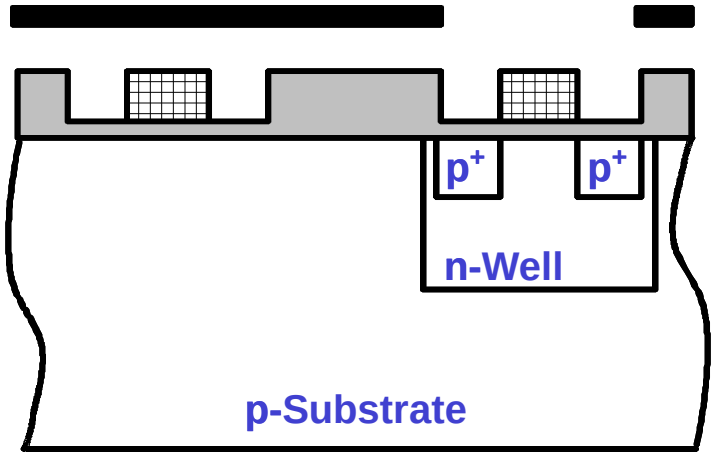
MOSFET Fabrication

c) Poly silicon

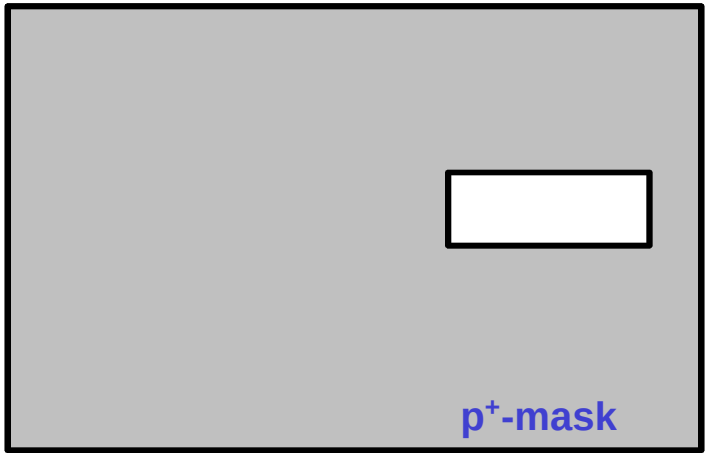




d) PMOS-Drain / Source

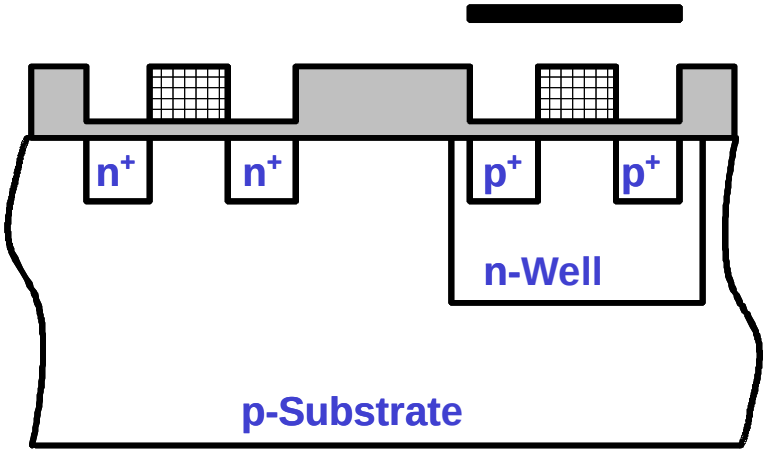


p-MOS Transistor

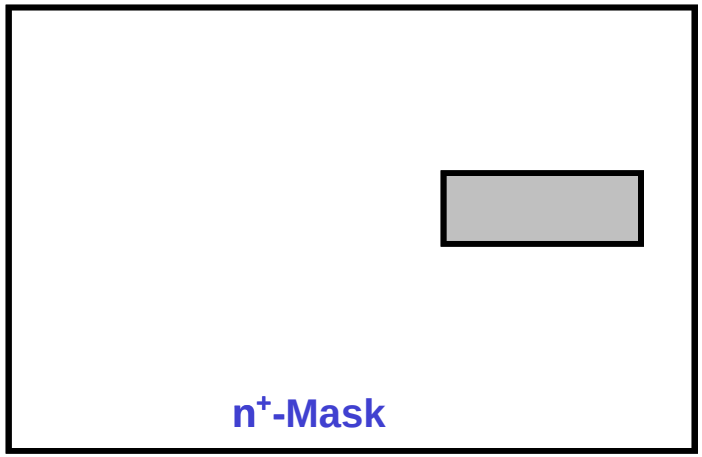


MOSFET Fabrication

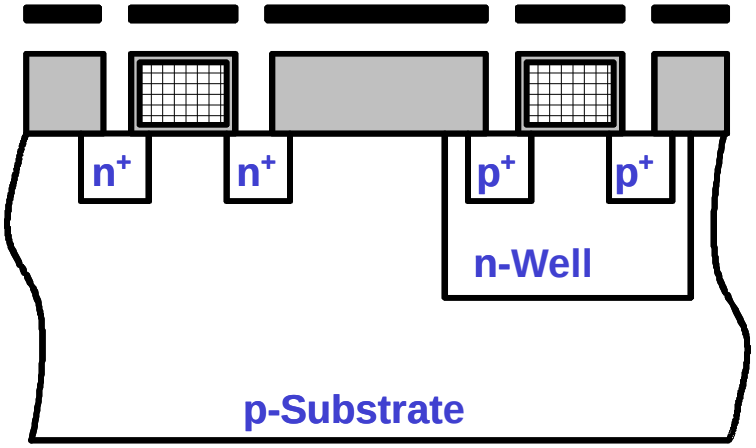
e) NMOS-Drain / Source

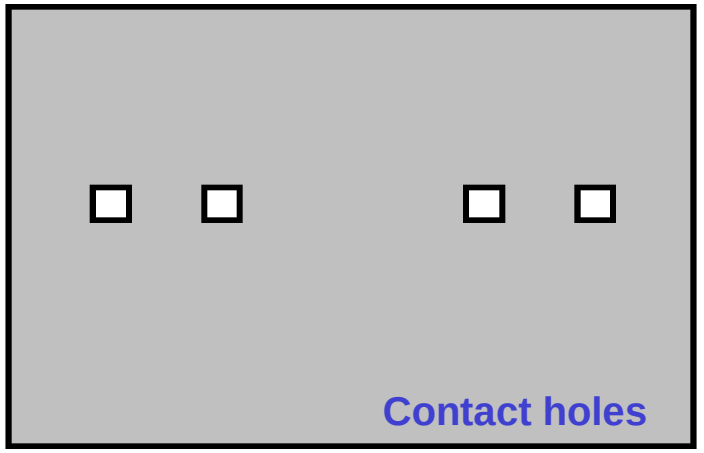


n-MOS Transistor



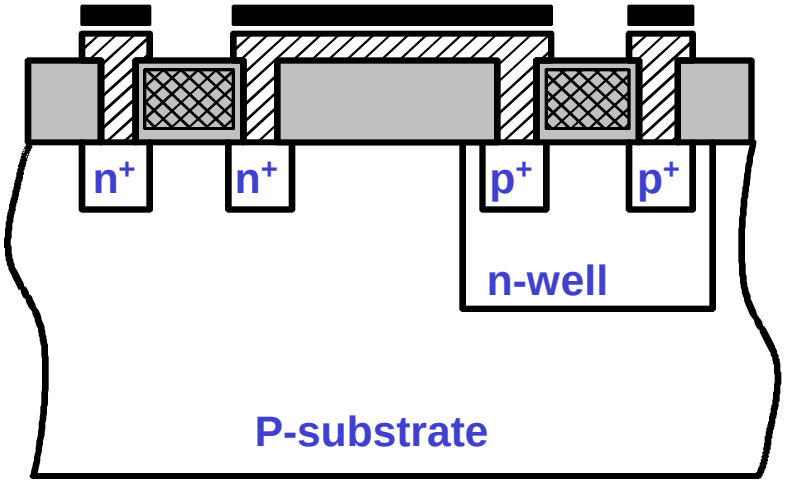
f) Contacts

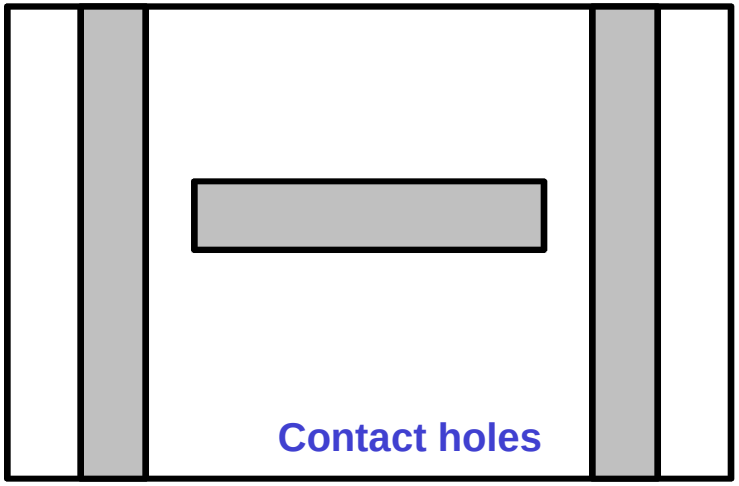




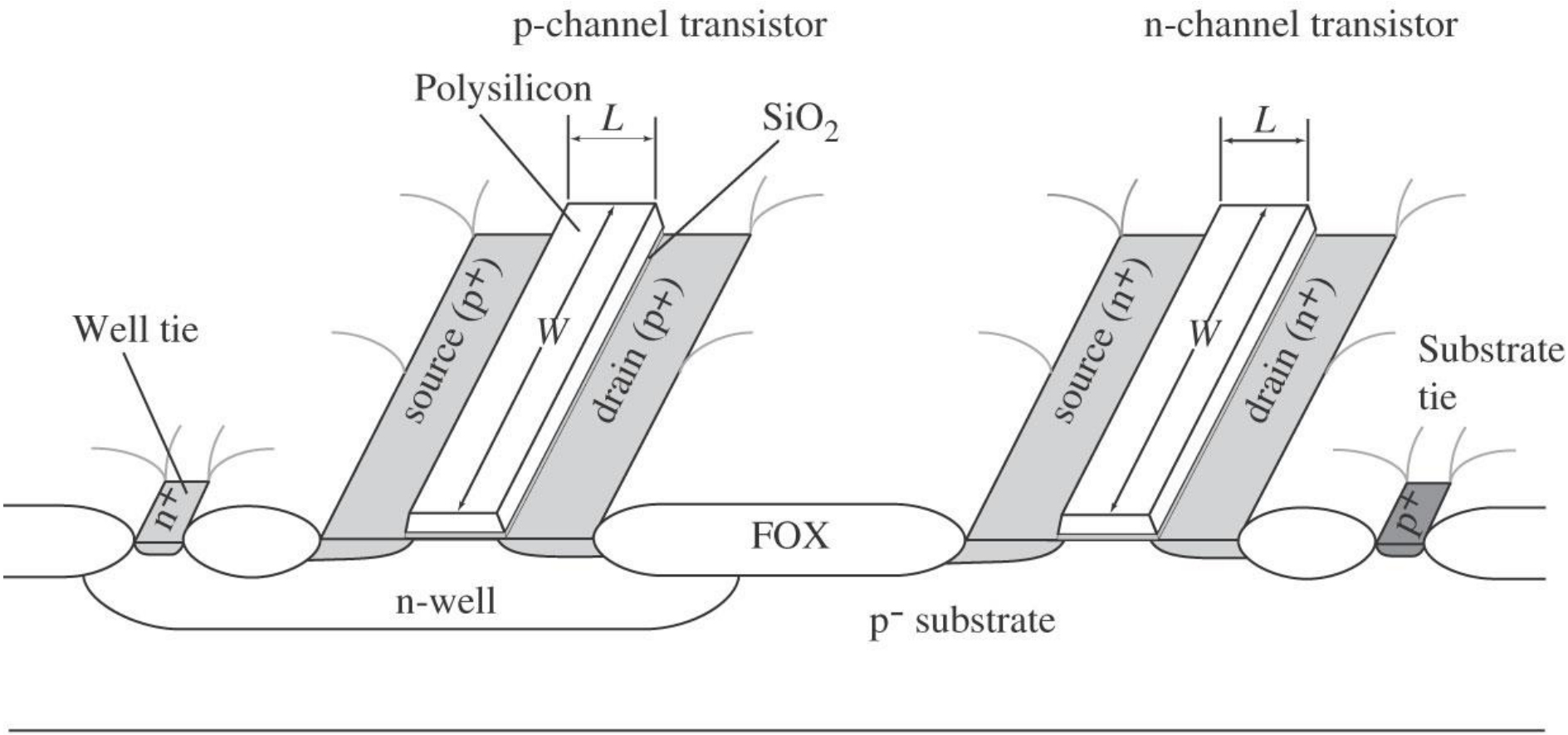
MOSFET Fabrication

g) Metal





MOSFET Structure



Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3\ \mu m$ in 0.6 μm process

Layout Design Rules

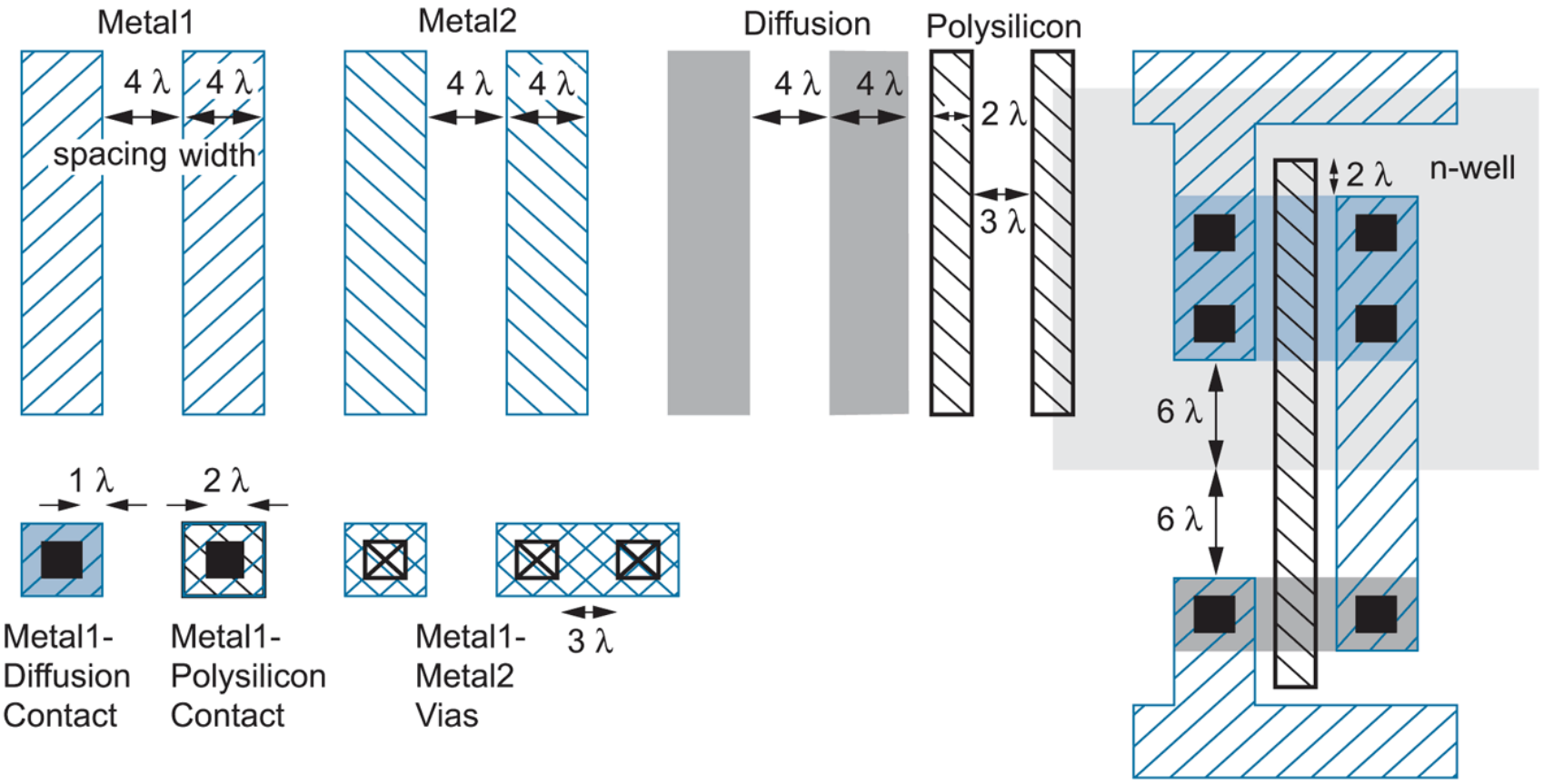


FIG 1.39 Simplified λ-based design rules

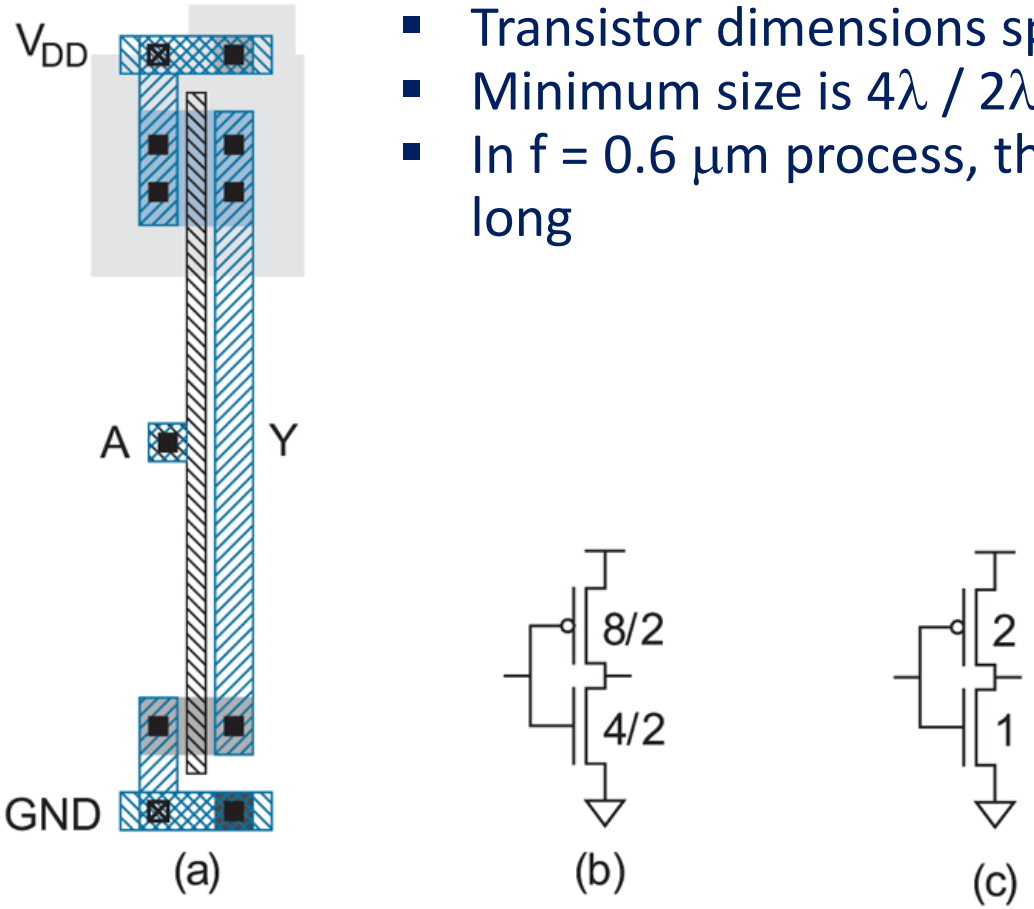
Design Rules Summary

- Metal and diffusion have minimum width and spacing of 4λ
- Contacts are 2λ x 2λ and must be surrounded by 1λ on the layers above and below
- Polysilicon uses a width of 2λ
- Polysilicon overlaps diffusions by 2λ where a transistor is desired and has spacing or 1λ away where no transistor is desired
- Polysilicon and contacts have a spacing of 3λ from other polysilicon or contacts
- N-well surrounds pMOS transistors by 6λ and avoid nMOS transistors by 6λ

Gate Layout

- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - VDD and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

Inverter Layout



- Transistor dimensions specified as W / L ratio
- Minimum size is 4λ / 2λ, sometimes called 1 unit
- In f = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long

FIG 1.40 Inverter with dimensions labeled

Example: Inverter Standard Cell Layout

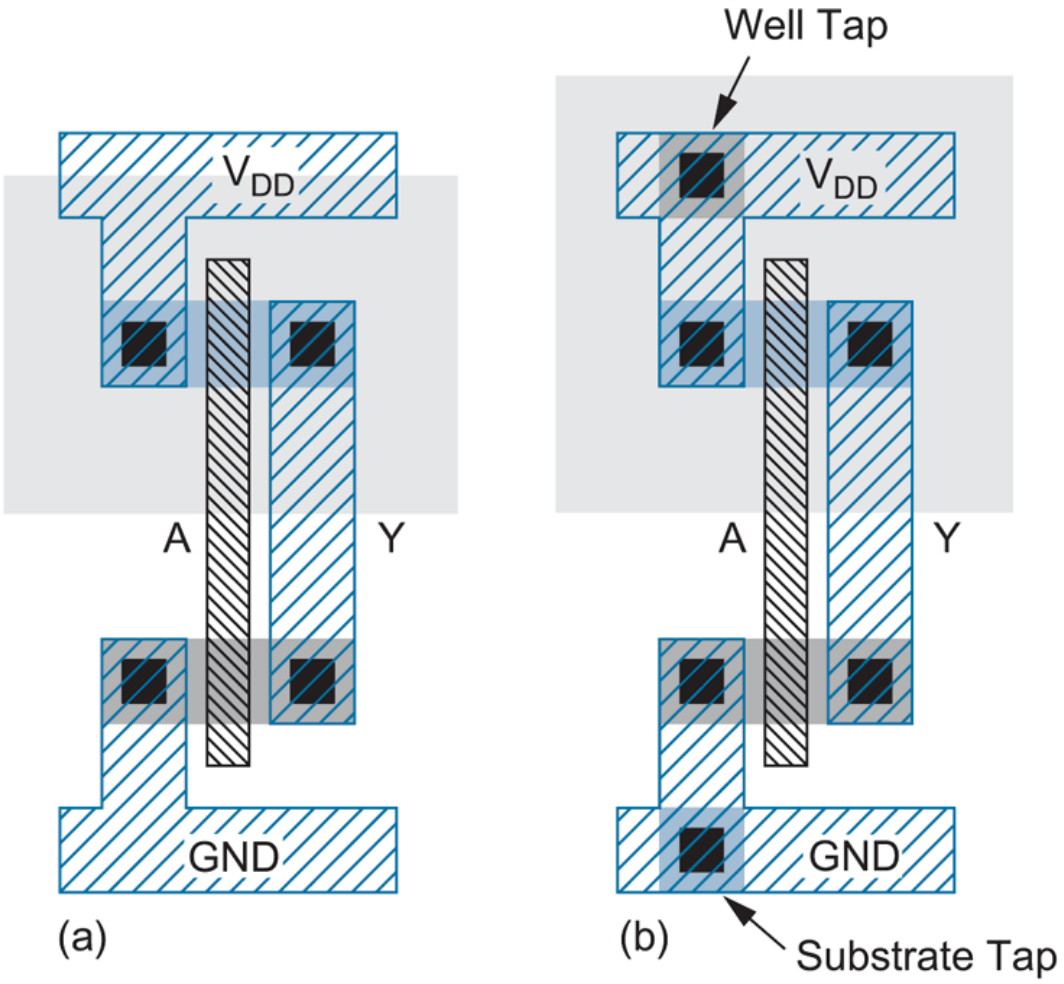
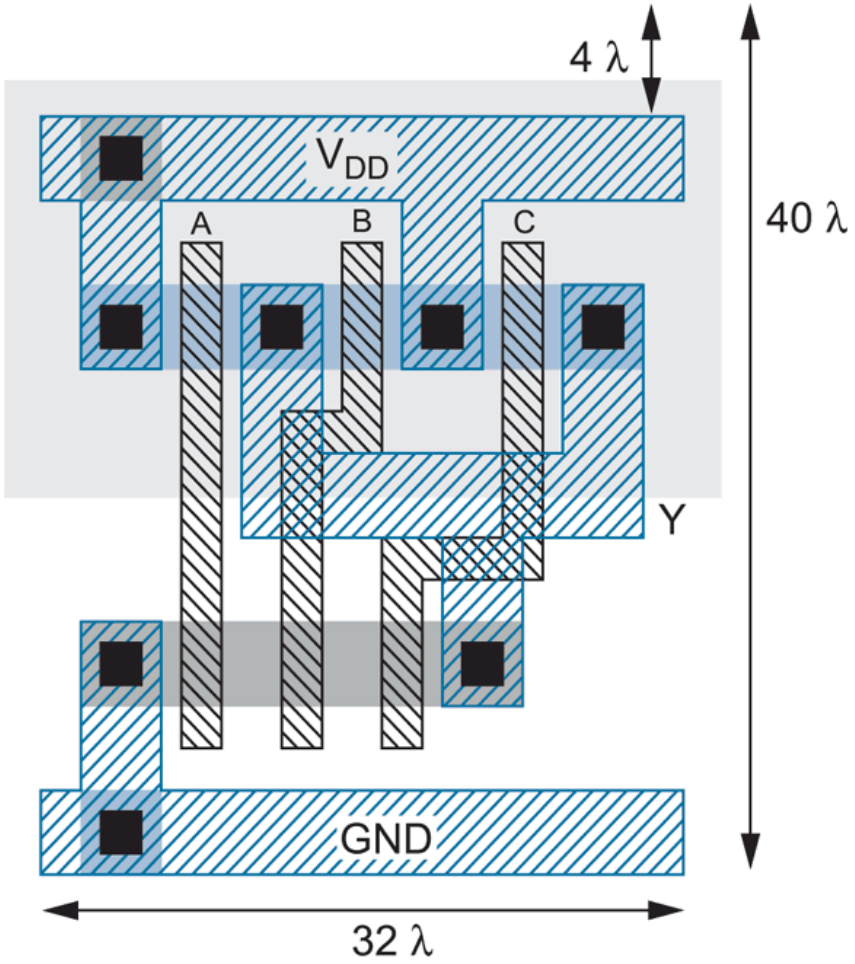


FIG 1.41 Inverter standard cell layout

Example: 3-input NAND Standard Cell Layout



- Horizontal n-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 VDD rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ

FIG 1.42 3-input NAND standard cell gate layouts

Stick Diagrams

- **Stick diagrams** help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

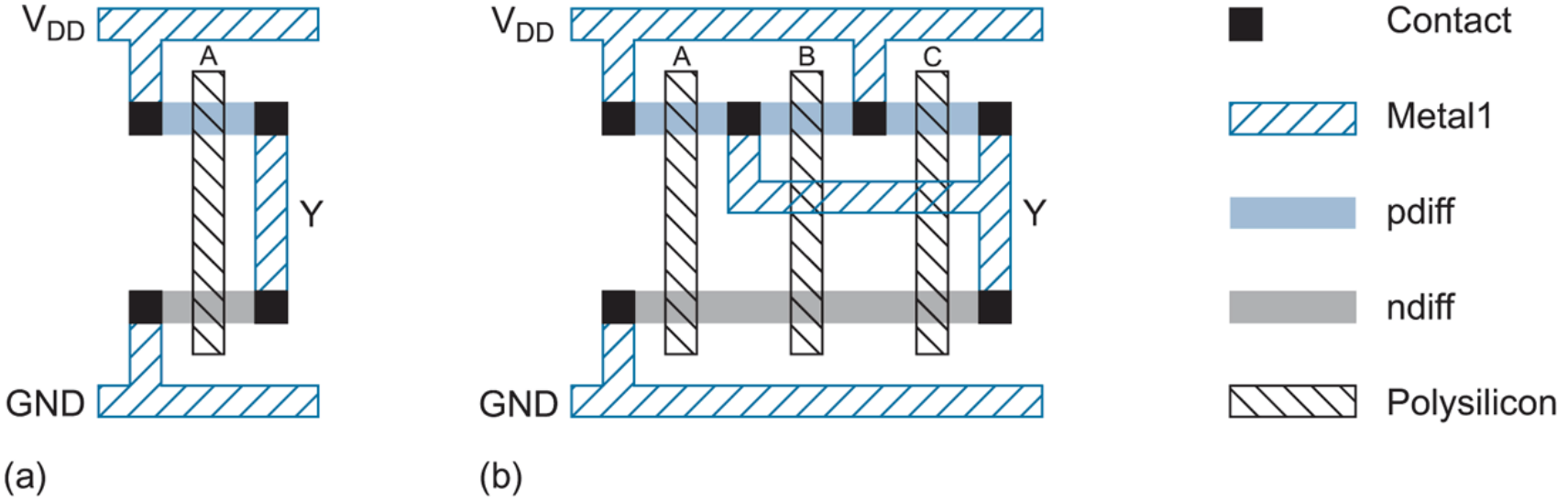


FIG 1.43 Stick diagrams of inverter and 3-input NAND gate. Color version on inside front cover.

Wiring Tracks

- A **wiring track** is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track

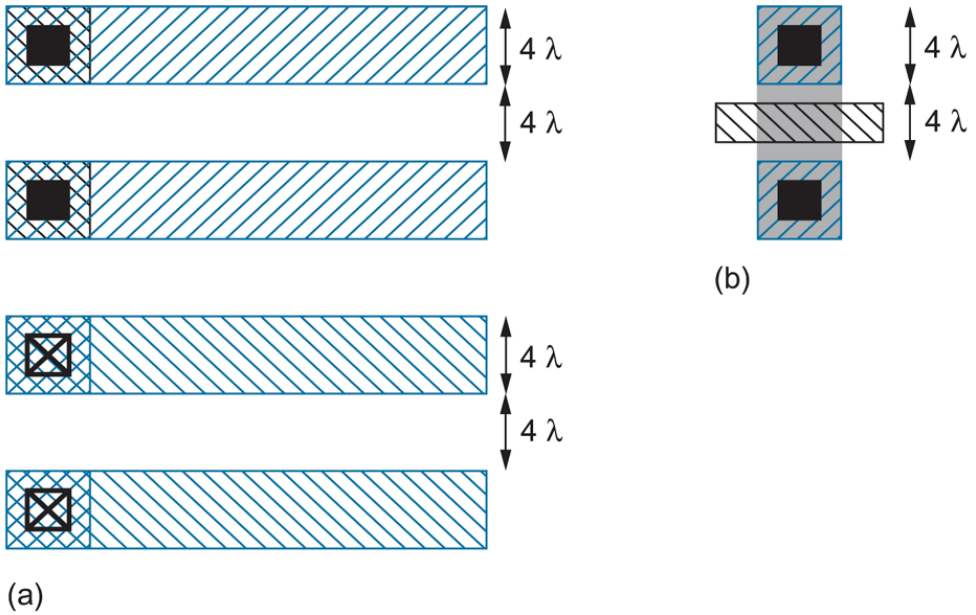


FIG 1.44 Pitch of routing tracks

Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track

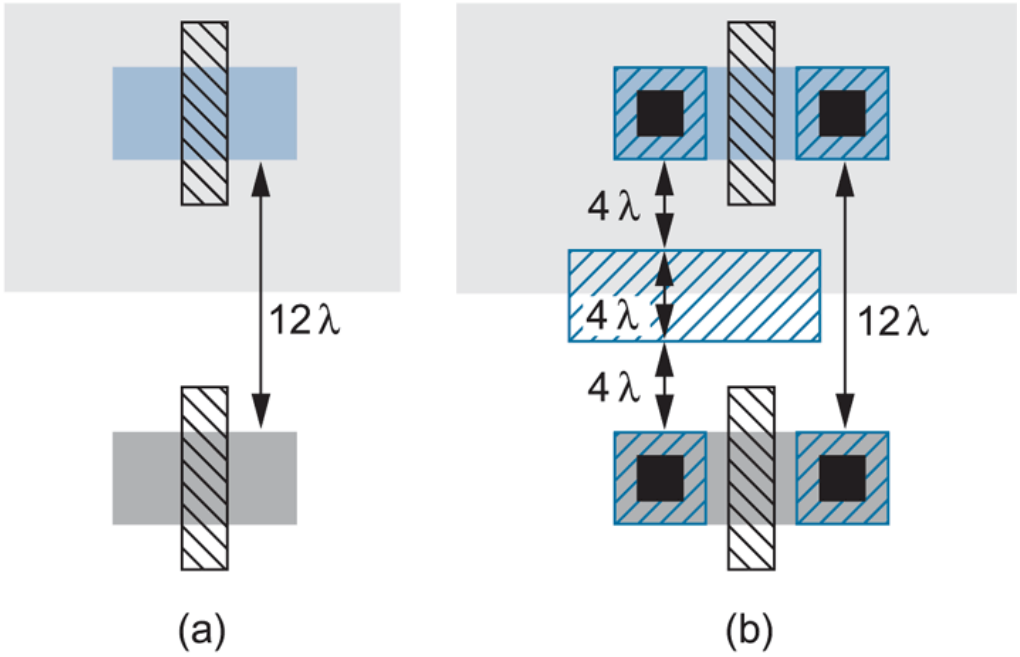


FIG 1.45 Spacing between nMOS and pMOS transistors

Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ

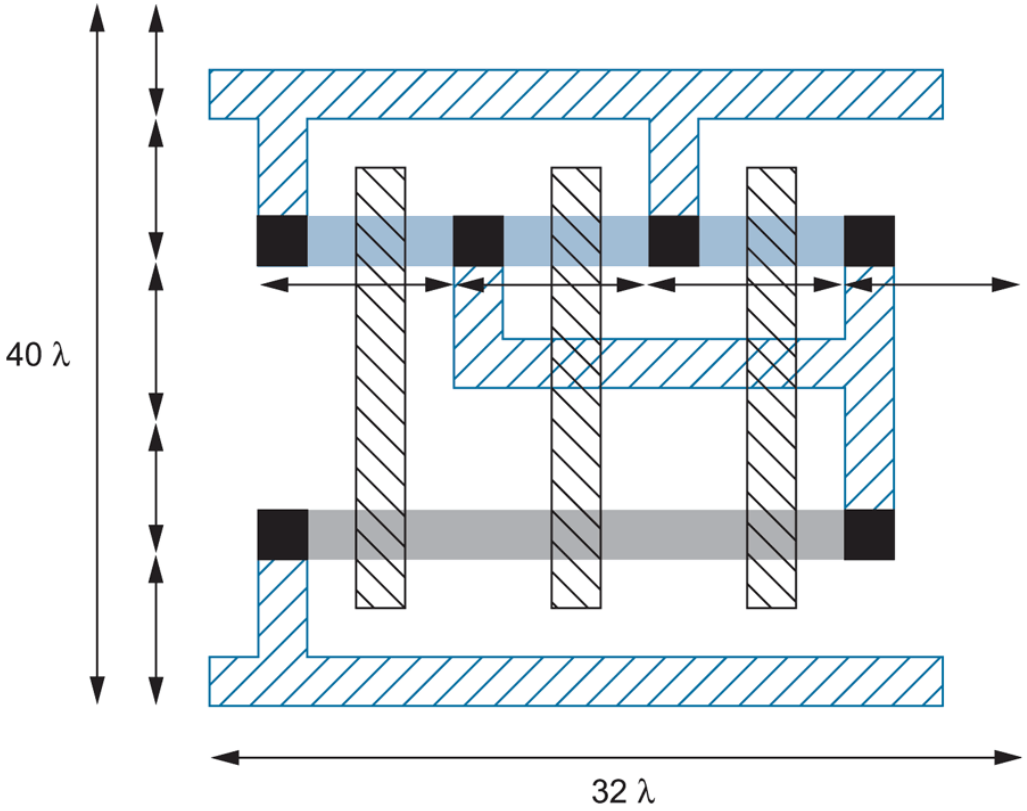
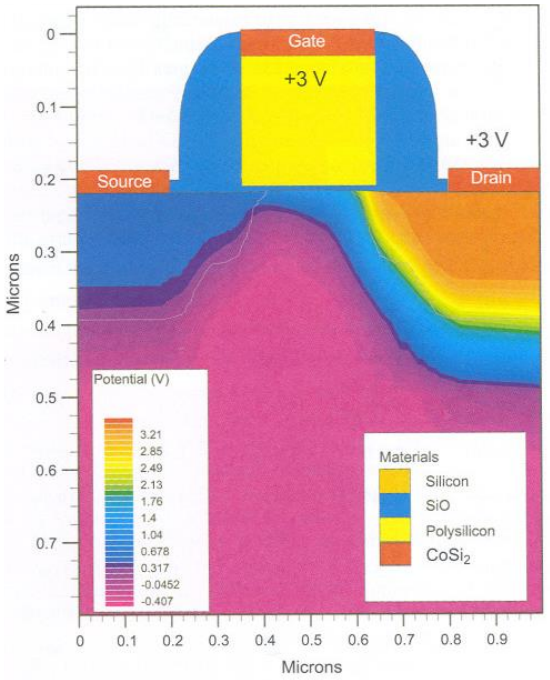


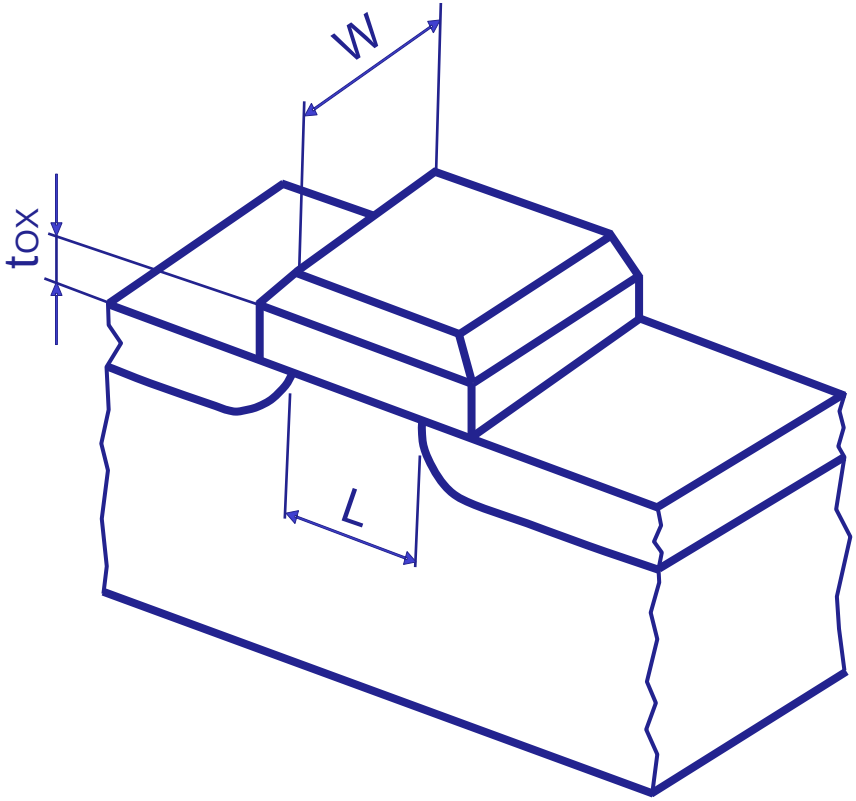
FIG 1.46 3-input NAND gate area estimation

Scaling

- The simplest and most common scaling approach is **constant field scaling**. The dimensions are scaled in the horizontal & vertical directions, and proportionally increasing the substrate doping by a factor λ, to keep the electric field distribution unchanged.
- One of the major changes in a short-channel device is that electric field in the channel region becomes two-dimensional due to the influence of the drain potential.
- The substrate doping has to be increased to decrease the depletion width (following from Poisson's equation).
- Small transistors have various undesired effects such as gate oxide degeneration due to 'hot' electrons, threshold voltage shift, gate-induced drain leakage, drain-induced barrier lowering (DIBL).
- Changes in the fabrication flow have to be introduced to mitigate these unwanted effects, and keep short-channel devices operational.



Constant Field Scaling



Parameter	Factor
Dimensions (W, L, t_{ox},…)	$1/\lambda$
Capacitors	$1/\lambda$
Voltages	$1/\lambda$
Currents	$1/\lambda$
Power	$1/\lambda^2$
Noise density (kT/C)	λ
SNR	$1/\lambda^3$

Constant Field Scaling

Parameter	Scaling Factor
Device Dimensions W, L, t_{OX}	$1/\lambda$
Capacitance C	$1/\lambda$
Line Resistance	λ
Contact Resistance	λ^2
Line Delay	1
Voltage V	$1/\lambda$
Current I	$1/\lambda$
Power P	$1/\lambda^2$
"On"-Resistance	1
Delay $T = R_{on}C$	$1/\lambda$
Power-Delay Product	$1/\lambda^3$
Transconductance g_m	1
Noise Power (kT/C)	λ
SNR	$1/\lambda^3$

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